36V_{IN}, 5A µModule Regulator with 5-Output Configurable LDO Array

FEATURES

- **Complete Step-Down Switch Mode Power Supply with Configurable Array of Five LDOs**
- **Step-Down Switching Power Supply**
  - **Adjustable 10% Accurate Output Current Limit**
  - **Constant-Current, Constant-Voltage Operation**
  - **Wide Input Voltage Range: 6V to 36V**
  - **1.2V to 24V Output Voltage**
- **Configurable Output LDO Array**
  - **Five 1.1A Parallelable Outputs**
  - **Outputs Adjustable from 0V to 24V**
  - **Low Output Noise: 90µV_{RMS} (100Hz to 1MHz)**
- 15mm × 15mm × 3.42mm Surface Mount BGA Package

APPLICATIONS

- FPGA, DSP, ASIC and Microprocessor Supplies
- Servers and Storage Devices
- RF Transceivers

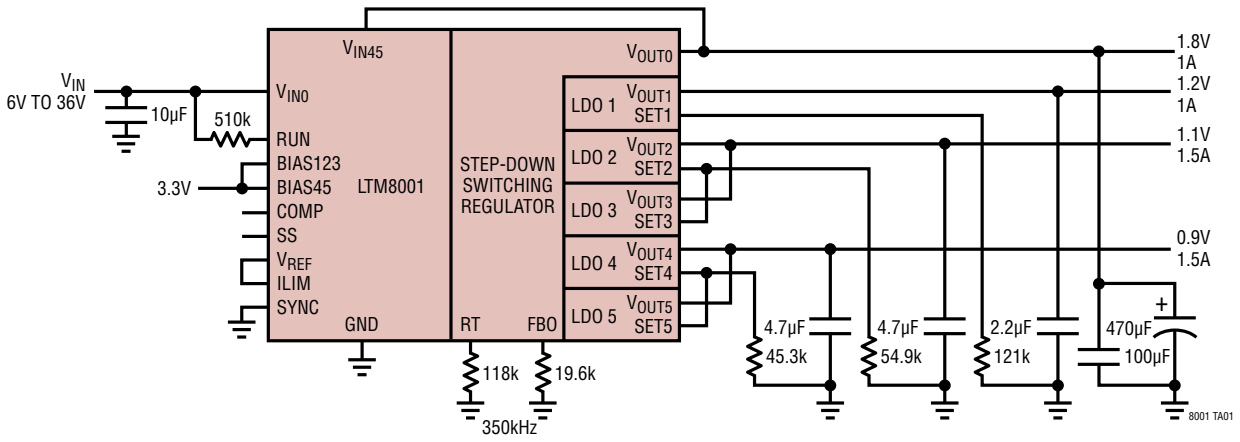
DESCRIPTION

The LTM®8001 is a 36V_{IN}, 5A step-down µModule® regulator with a 5-output configurable LDO array. Operating over an input voltage range of 6V to 36V, the LTM8001 buck regulator supports an output voltage range of 1.2V to 24V. Following the buck regulator is an array of five 1.1A linear regulators whose outputs may be connected in parallel to accommodate a wide variety of load combinations. Three of these LDOs are tied to the output of the buck regulator, while the other two are tied together to an undedicated input.

The low profile package (3.42mm) enables utilization of unused space on the bottom of PC boards for high density point of load regulation. The LTM8001 is packaged in a thermally enhanced, compact (15mm × 15mm) and low profile (3.42mm) overmolded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8001 is available with SnPb (BGA) or RoHS compliant terminal finish.

TYPICAL APPLICATION

5A Output DC/DC µModule Converter

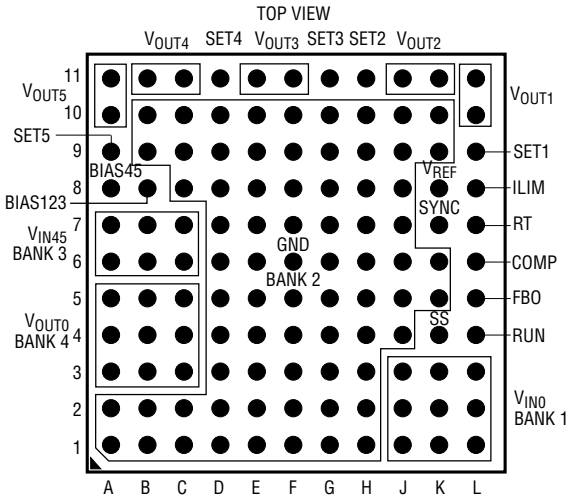


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN0} 40V
V_{IN45}, BIAS45 ..... 25V
BIAS123 ..... 25V
FB0, RT, COMP, ILIM, V_{REF} 3V
V_{OUT0-5} 25V
RUN, SYNC, SS 6V
SET1-5 (Relative to V_{OUT1-5}, Respectively) ..... ±0.3V
Current Into SET1-5 ..... ±10mA
Current Into RUN Pin 100µA
Maximum Junction Temperature (Notes 2, 3) ..... 125°C
Peak Solder Reflow Body Temperature ..... 245°C
Storage Temperature ..... –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
121 PADS (15mm × 15mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 16.1°C/W, $\theta_{JCbottom}$ = 5.99°C/W, θ_{JCtop} = 13.4°C/W, θ_{JB} = 4.98°C/W
θ VALUES DETERMINED PER JESD 51-9, 51-12
WEIGHT = 1.8 GRAMS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM8001EY#PBF	SAC305 (RoHS)	LTM8001Y	e1	BGA	3	–40°C to 125°C
LTM8001IY#PBF	SAC305 (RoHS)	LTM8001Y	e1	BGA	3	–40°C to 125°C
LTM8001IY	SnPb (63/37)	LTM8001Y	e0	BGA	3	–40°C to 125°C
LTM8001MPY#PBF	SAC305 (RoHS)	LTM8001Y	e1	BGA	3	–55°C to 125°C
LTM8001MPY	SnPb (63/37)	LTM8001Y	e0	BGA	3	–55°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is indicated by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 3V unless otherwise noted (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck Regulator						
Minimum V_{IN0} Input Voltage		●			6	V
V_{OUT0} Output DC Voltage	0A < I_{OUT} ≤ 3A, R_{FB0} Open 0A < I_{OUT} ≤ 3A; R_{FB0} = 536Ω			1.2 24		V V
V_{OUT0} Output DC Current	6V < V_{IN0} < 36V, V_{OUT} = 3.3V		0		5	A
Quiescent Current Into V_{IN0}	RUN = 0V No Load			0.1 26	1 40	µA mA
V_{OUT0} Line Regulation	6V < V_{IN0} < 36V, I_{OUT} = 1A			±0.5		%
V_{OUT0} Load Regulation	V_{IN0} = 24V, 0A < I_{OUT} < 5A			±1.2		%
V_{OUT0} RMS Voltage Ripple	V_{IN0} = 24V, I_{OUT} = 5A			10		mV
Switching Frequency	R_T = 39.2k R_T = 200k			1000 200		kHz kHz
Voltage at FB0 Pin		●	1.15	1.19	1.21	V
Internal FBO Resistor				10		kΩ
RUN Pin Current	RUN = 1.45V			5.5		µA
RUN Threshold Voltage (Falling)			1.49		1.61	V
RUN Threshold Voltage (Rising)			1.63		1.75	V
ILIM Control Range			0		1.5	V
ILIM Pin Current				100		nA
ILIM Current Limit Accuracy	ILIM = 1.5V ILIM = 0.75V		5.1 2.5		6.4 3.4	A A
V_{REF} Voltage	0.5mA Load		1.9	2	2.1	V
SS Pin Current				11		µA
SYNC Input Low Threshold	f_{SYNC} = 500kHz		0.8			V
SYNC Input High Threshold	f_{SYNC} = 500kHz				1.2	V
SYNC Input Current	SYNC = 0V SYNC = 2V		–0.1		 0.1	µA µA
LDO Array						
SET1-5 Pin Current	BIAS123 = BIAS45 = 2V, SETx = 0V, I_{OUT1-5} = 1mA	 ●	9.85 9.80	10 10	10.15 10.20	µA µA
V_{OUTx} – SETx Offset Voltage	BIAS123 = BIAS45 = 2V, SETx = 0V, I_{OUT1-5} = 1mA	 ●	–4 –6.5		4 6.5	mV mV
Line Regulation for SET Current	1V < V_{OUT0} = V_{IN45} < 22V, I_{OUTx} = 1mA (Note 4)	●			11	nA
Line Regulation for V_{OUT1-5}	1V < V_{OUT0} = V_{IN45} < 22V, I_{OUTx} = 1mA (Note 4)			0.25		mV
Load Regulation for SETx Current	I_{OUT1-5} = 1mA to 1.1A				25	nA
Load Regulation for V_{OUT1-5}	I_{OUT1-5} = 1mA to 1.1A	 ●			34 52	mV mV
Minimum Load Current for V_{OUT1-5} (Note 4)	V_{OUT0} = V_{IN45} = BIAS123 = BIAS45 = 10V V_{OUT0} = V_{IN45} = BIAS123 = BIAS45 = 22V	● ●			500 1	µA mA
BIAS123, BIAS45 Dropout Voltage	I_{OUT1-5} = 100mA I_{OUT1-5} = 1.1A	 ●		1.2	 1.6	V V
V_{OUT0} to V_{OUT1-3} and V_{IN45} to V_{OUT4-5} Dropout Voltage	I_{OUT1-5} = 100mA I_{OUT1-5} = 1.1A	 ●		100	 500	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 3V unless otherwise noted (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum V_{OUT0} to V_{OUT1-3} and V_{IN45} to V_{OUT4-5} Differential Voltage (Note 5)	I_{OUT1-5} = 310mA I_{OUT1-5} = 125mA				15 22	V V
BIAS123, BIAS45 Pin Current	I_{OUT1-5} = 100mA I_{OUT1-5} = 1.1A	 ●			6 30	mA mA
V_{OUT1-5} Current Limit (Note 5)	V_{OUT1-5} = –0.1V			1.3		A
V_{OUT1-5} RMS Output Noise	V_{OUT1-5} = 1V, I_{OUT1-5} = 1.1A, 100Hz to 1MHz			90		μV_{RMS}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This µModule regulator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LTM8001E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8001I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8001MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

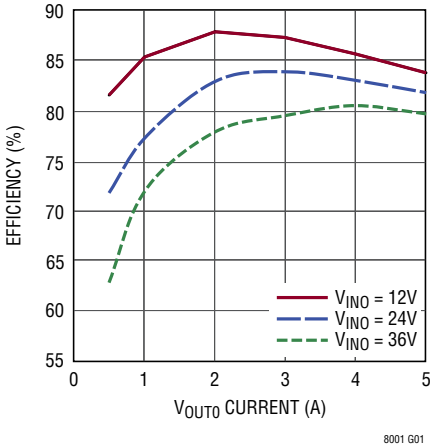
Note 4: No minimum load is required if the respective linear regulator is off, such as when V_{OUT0} = 0V, V_{IN45} = 0V, BIAS123 = 0V or BIAS45 = 0V.

Note 5: The current limit may decrease to zero at input-to-output differential voltages greater than 22V. Operation at voltages for V_{OUT0}, V_{IN45}, BIAS123 and BIAS45 is allowed up to a maximum of 25V as long as the difference between the linear regulator input and output voltage is below the specified differential voltage. Line and load regulation specifications are not applicable when the device is in current limit.

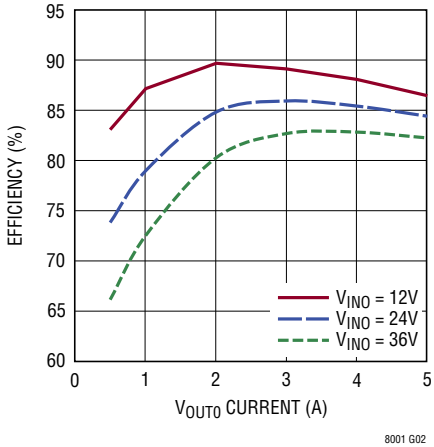
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Configured per Table 1, where applicable.)

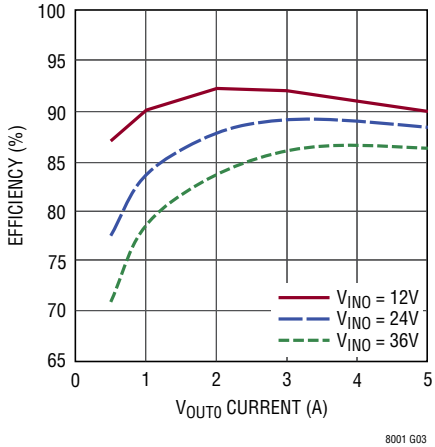
Efficiency vs Output Current, V_{OUT0} = 2.5V, f_{SW} = 450kHz



Efficiency vs Output Current, V_{OUT0} = 3.3V, f_{SW} = 550kHz



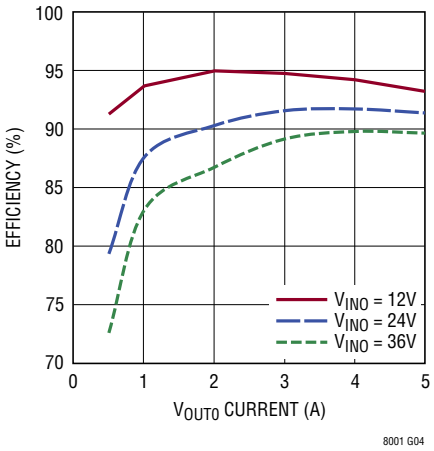
Efficiency vs Output Current, V_{OUT0} = 5V, f_{SW} = 600kHz



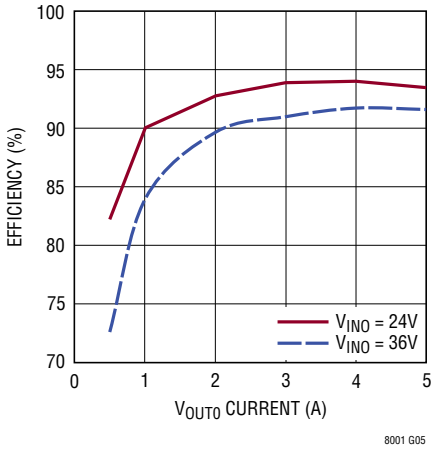
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Configured per Table 1, where applicable.)

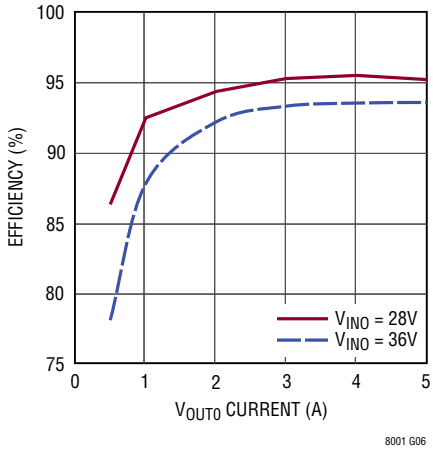
Efficiency vs Output Current, V_{OUT0} = 8V, f_{SW} = 625kHz



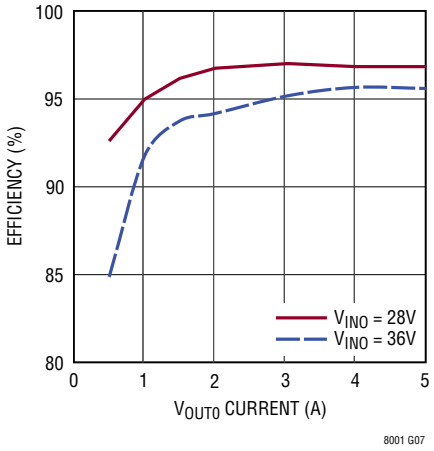
Efficiency vs Output Current, V_{OUT0} = 12V, f_{SW} = 650kHz



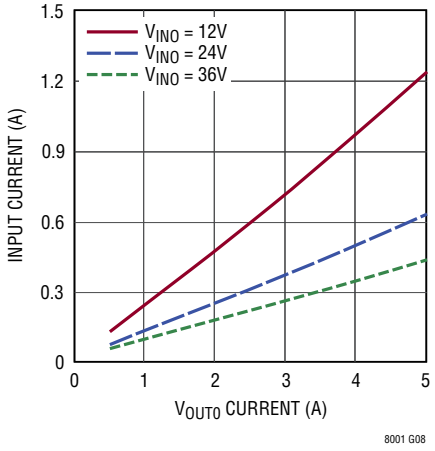
Efficiency vs Output Current, V_{OUT0} = 18V, f_{SW} = 675kHz



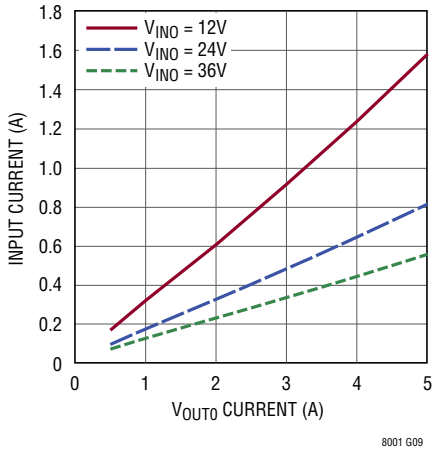
Efficiency vs Output Current, V_{OUT0} = 24V, f_{SW} = 700kHz



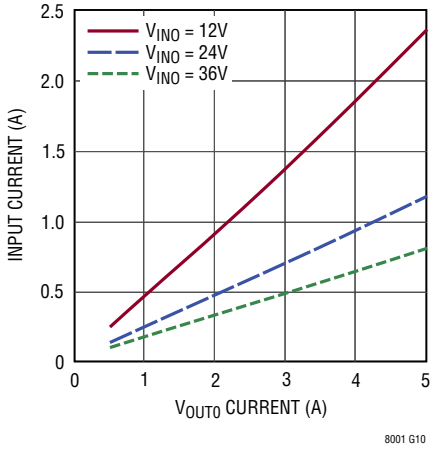
Input Current vs Output Current, V_{OUT0} = 2.5V



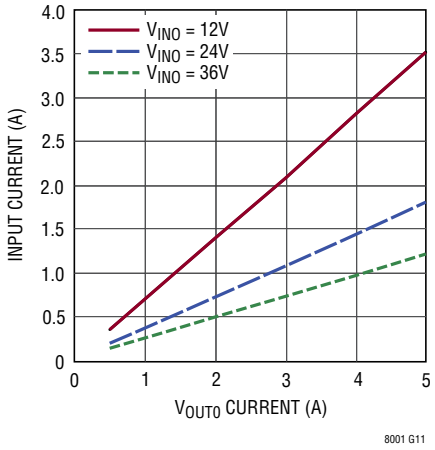
Input Current vs Output Current, V_{OUT0} = 3.3V



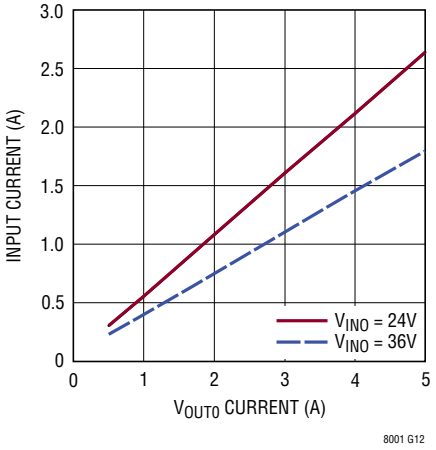
Input Current vs Output Current, V_{OUT0} = 5V



Input Current vs Output Current, V_{OUT0} = 8V



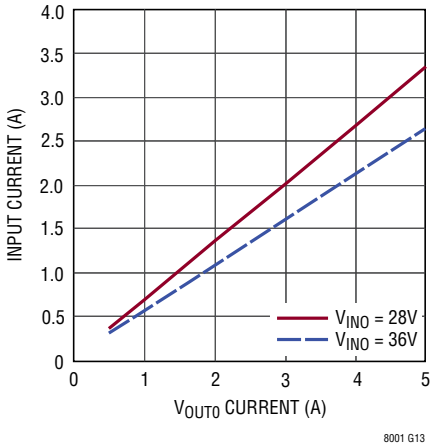
Input Current vs Output Current, V_{OUT0} = 12V



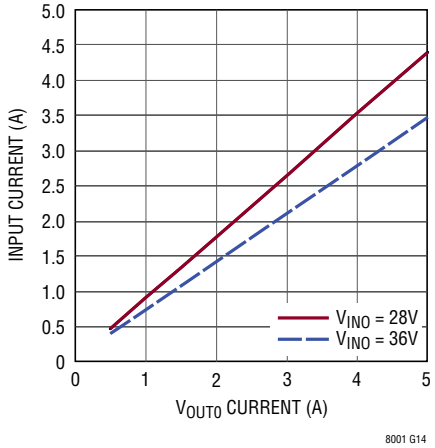
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Configured per Table 1, where applicable.)

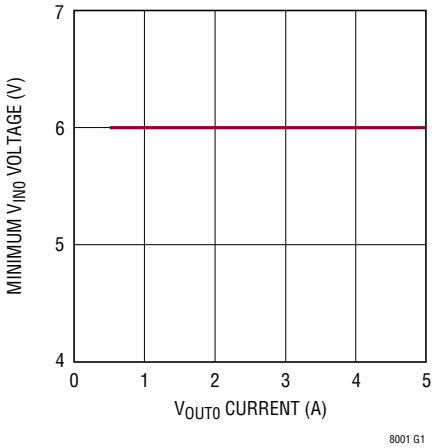
Input Current vs Output Current, V_{OUT0} = 18V



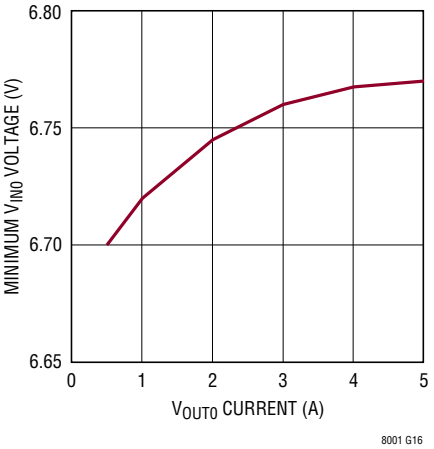
Input Current vs Output Current, V_{OUT0} = 24V



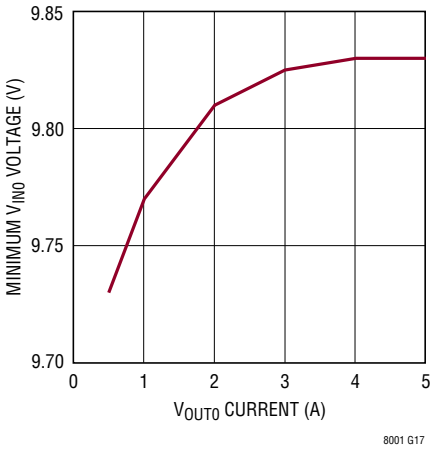
Minimum V_{INO} vs Output Current, V_{OUT0} = 3.3V and Below



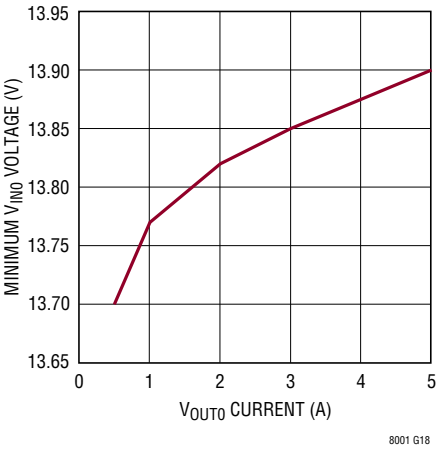
Minimum V_{INO} vs Output Current, V_{OUT0} = 5V



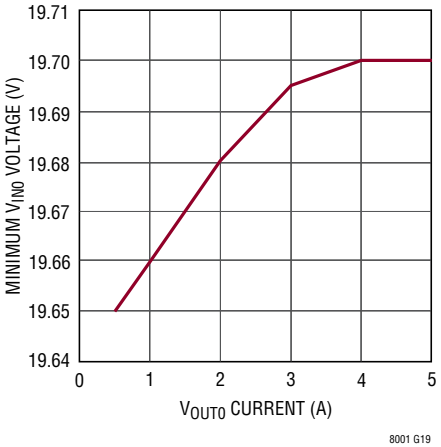
Minimum V_{INO} vs Output Current, V_{OUT0} = 8V



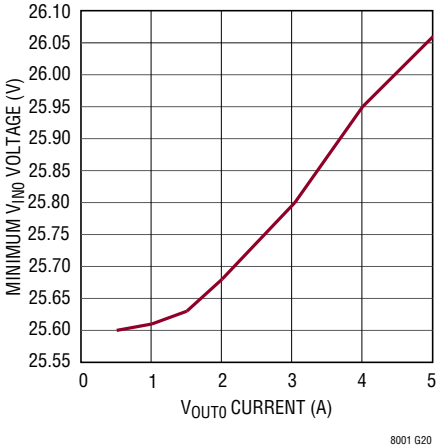
Minimum V_{INO} vs Output Current, V_{OUT0} = 12V



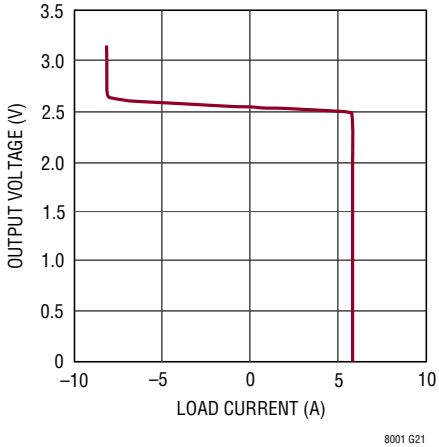
Minimum V_{INO} vs Output Current, V_{OUT0} = 18V



Minimum V_{INO} vs Output Current, V_{OUT0} = 24V



Output Voltage vs Output Current, V_{OUT0} = 2.5V

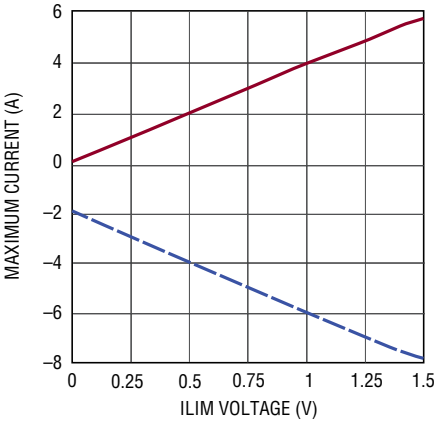


Rev. E

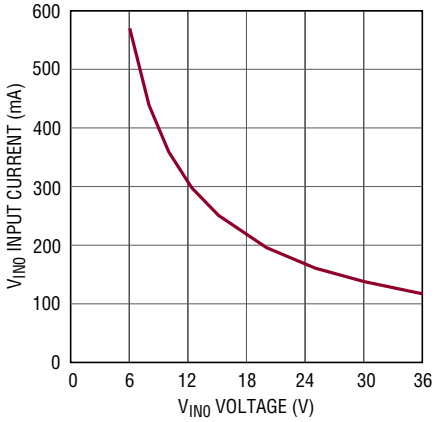
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Configured per Table 1, where applicable.)

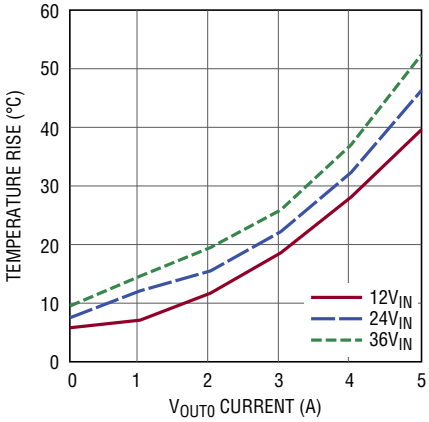
ILIM Voltage vs Maximum I_{OUT0} Output Current



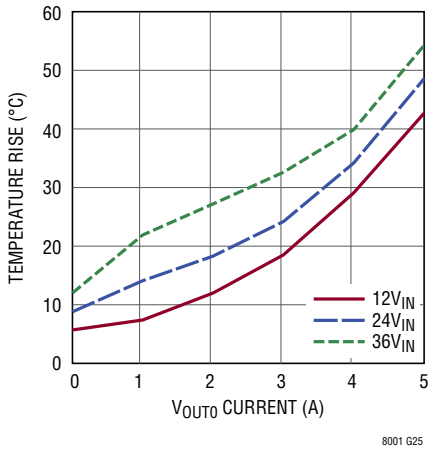
V_{IN0} Input Current vs Voltage, V_{OUT0} Shorted



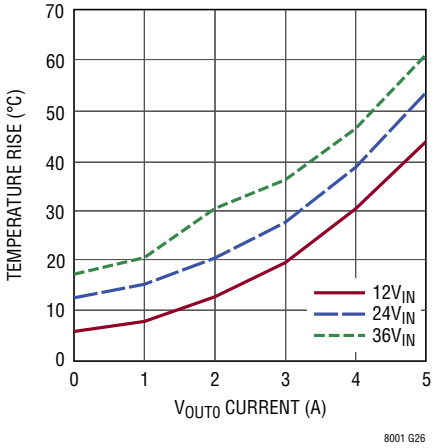
Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 2.5V



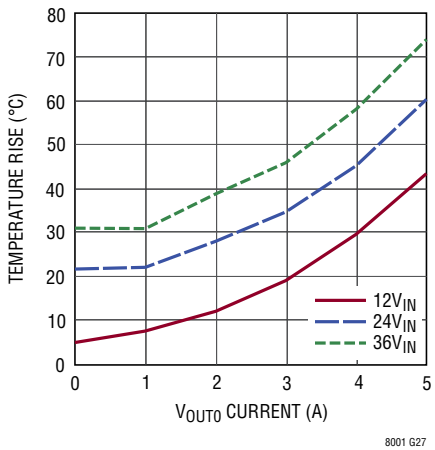
Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 3.3V



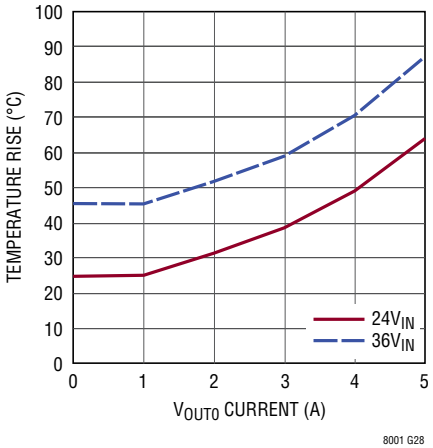
Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 5V



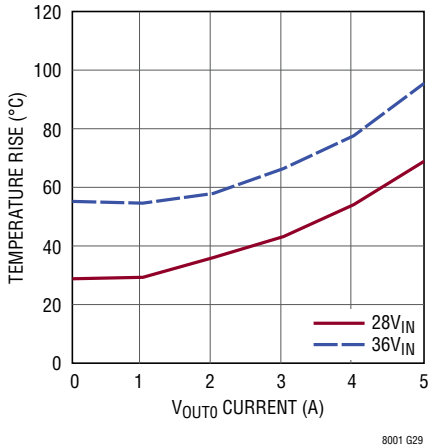
Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 8V



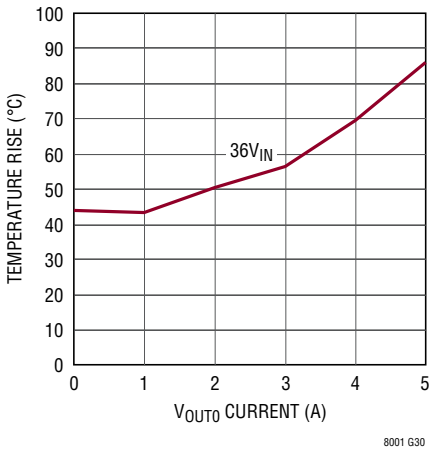
Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 12V



Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 18V



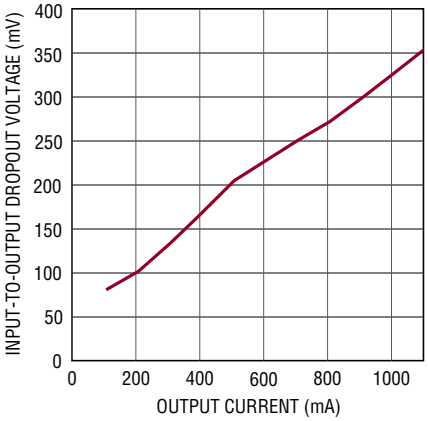
Temperature Rise vs V_{OUT0} Current, Buck Regulator, V_{OUT0} = 24V



TYPICAL PERFORMANCE CHARACTERISTICS

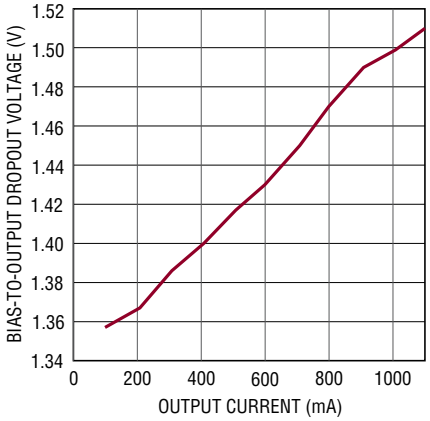
(T_A = 25°C unless otherwise noted. Configured per Table 1, where applicable.)

LDO Input-to-Output Dropout Voltage vs Output Current



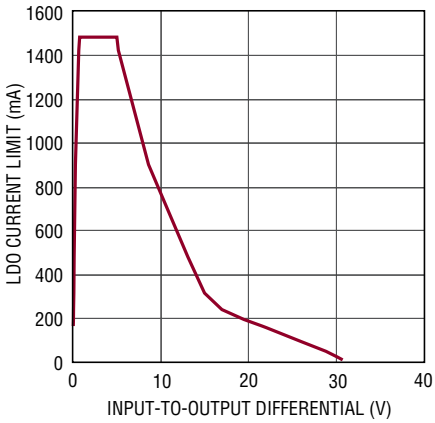
8001 G31

LDO V_{BIAS}-to-Output Dropout Voltage vs Output Current



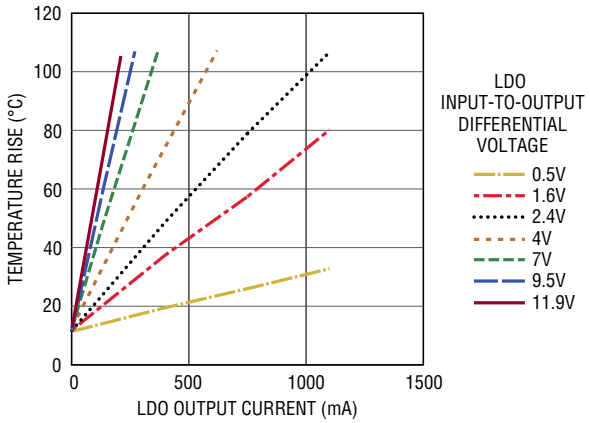
8001 G32

LDO Current Limit vs Input-to-Output Differential Voltage



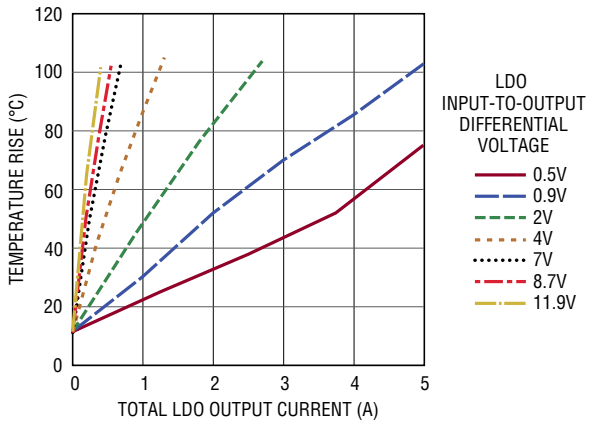
8001 G33

LDO Temperature Rise vs LDO Output Current (V_{IN} = 24V, V_{OUT0} = 12V, 1 LDO Powered)



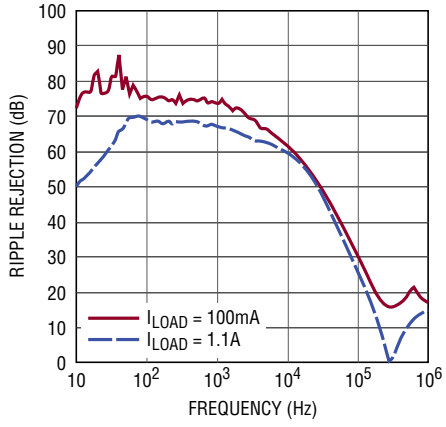
8001 G34

LDO Temperature Rise vs LDO Output Current (V_{IN} = 24V, V_{OUT0} = 12V, 5 LDOs in Parallel)



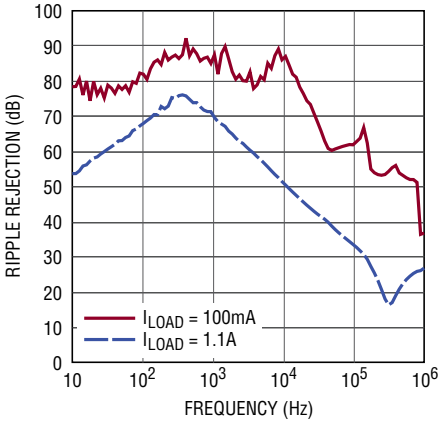
8001 G35

LDO Input Voltage Ripple Rejection (V_{OUT4} = 2.5V, V_{IN45} = V_{BIAS45} = 4.5V)



8001 G36

LDO Input Voltage Ripple Rejection (V_{OUT4} = 2.5V, V_{BIAS45} = 4.5V, V_{IN45} = 3.5V)

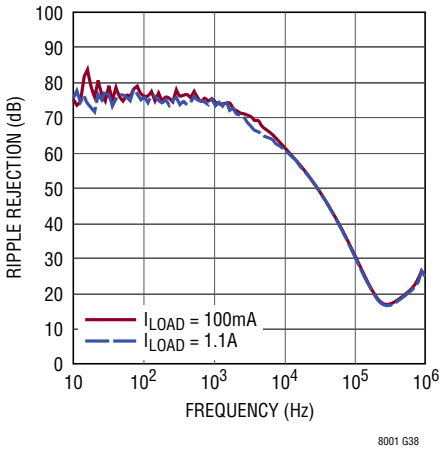


8001 G37

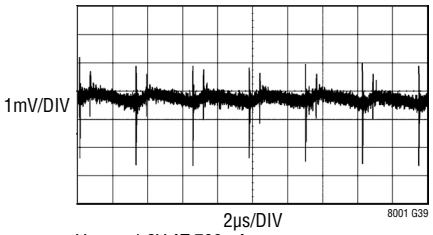
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Configured per Table 1, where applicable.)

LDO V_{BIAS} Ripple Rejection (V_{OUT4} = 2.5V, V_{BIAS45} = 4.5V, V_{IN45} = 3.5V)



LDO Output Ripple



V_{OUT} = 1.2V AT 700mA
C_{OUT1} = 22µF
C_{SET1} = 1nF
V_{IN} = 12V
V_{OUT0} = 1.8V LOADED TO A TOTAL CURRENT OF 5A
100MHz BW

PIN FUNCTIONS

V_{IN0} (Bank 1): The V_{IN0} bank supplies current to the LTM8001's internal regulator and to the internal power switches. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8001 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8001 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{FB0}) to this net.

V_{IN45} (Bank 3): Input to the LDOs connected to V_{OUT4} and V_{OUT5}. It must be locally bypassed with a low ESR capacitor.

V_{OUT0} (Bank 4): Switching Power Converter Output Pins. Apply the output filter capacitor and the output load between these pins and the GND pins. In most cases, an output capacitance made up of a combination of ceramic and electrolytic capacitors yields the optimal volumetric solution.

BIAS45 (Pin A8): This pin is the supply pin for the control circuitry of the LDOs connected to V_{OUT4} and V_{OUT5}. For the LDOs to regulate, this voltage must be more than 1.2V to 1.6V greater than the output voltage (see Dropout specifications).

BIAS123 (Pin B8): This pin is the supply pin for the control circuitry of the LDOs connected to V_{OUT1}-V_{OUT3}. For the LDOs to regulate, this voltage must be more than 1.2V to 1.6V greater than the output voltage (see Dropout specifications).

SS (Pin K4): The Soft-Start Pin. Place an external capacitor to ground to limit the regulated current during start-up conditions. The soft-start pin has an 11µA charging current.

SYNC (Pin K7): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. This pin should be grounded when not in use. Do not leave this pin floating. When laying out the board, avoid noise coupling to or from the SYNC trace. See the Switching Frequency Synchronization section in Applications Information.

V_{REF} (Pin K8): Buffered 2V Reference Capable of 0.5mA Drive.

RUN (Pin L4): The RUN pin acts as an enable pin and turns on the internal circuitry. The pin does not have any pull up or pull down, requiring a voltage bias for normal part operation. The RUN pin is internally clamped, so it may be pulled up to a voltage source that is higher than

PIN FUNCTIONS

the absolute maximum voltage rating of 6V through a resistor, provided the pin current does not exceed 100µA.

FB0 (Pin L5): The LTM8001 regulates its FB0 pin to 1.19V. Connect the adjust resistor from this pin to ground. The value of R_{FB0} is given by the equation:

$$R_{FB0} = \frac{11.9}{V_{OUT} - 1.19}$$

where R_{FB0} is in kΩ.

COMP (Pin L6): Compensation Pin. This pin is generally not used. The LTM8001 is internally compensated, but some rare situations may arise that require a modification to the control loop. This pin connects directly to the input PWM comparator of the LTM8001. In most cases, no adjustment is necessary. If this function is not used, leave this pin open.

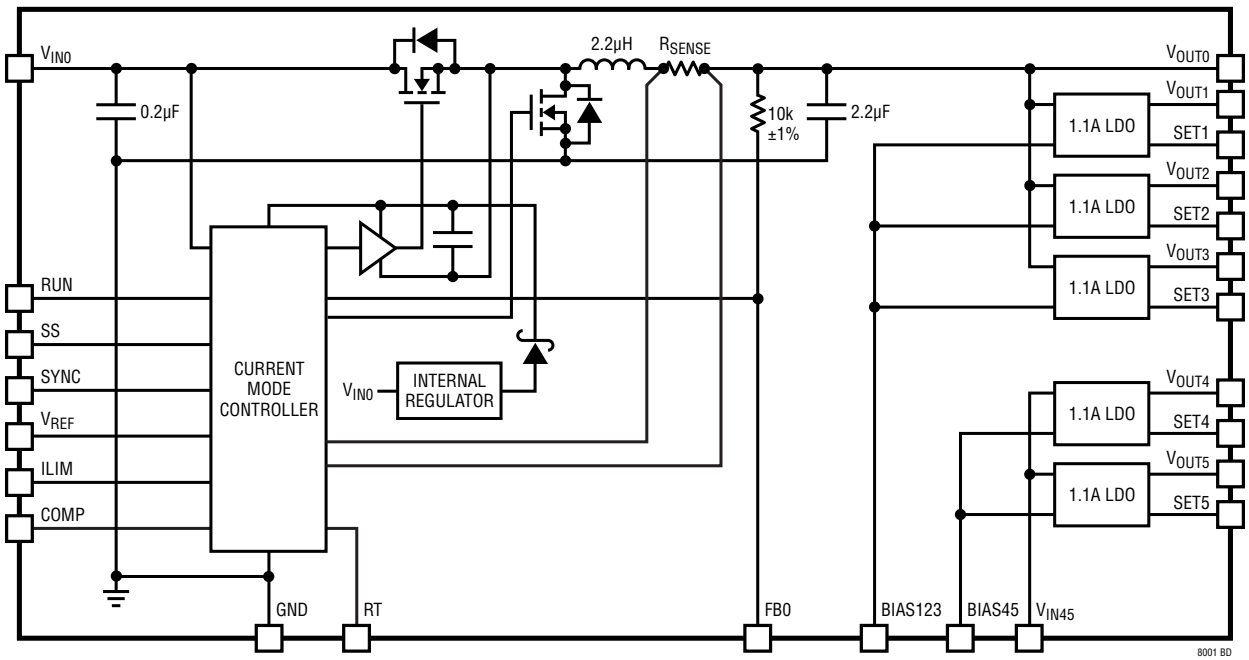
RT (Pin L7): The RT pin is used to program the switching frequency of the LTM8001 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the recommended resistance value and switching frequency. When using the SYNC function, set the frequency to be 20% lower than the SYNC pulse frequency. Do not leave this pin open.

ILIM (Pin L8): The ILIM pin reduces the maximum regulated output current of the LTM8001. The maximum control voltage range is 1.5V. ILIM voltages above 1.5V have little or no effect. If this function is not used, tie this pin to V_{REF}.

SET1, SET2, SET3, SET4, SET5 (Pins L9, H11, G11, D11, A9): These pins set the regulation point for each LDO. A fixed current of 10µA flows out of this pin through a single external resistor, which programs the output voltage of the device. Output voltage range is zero to the absolute maximum rated output voltage. The transient performance can be improved by adding a small capacitor from the SET pin to ground.

V_{OUT1} (Pins L10, L11), V_{OUT2} (Pins J11, K11), V_{OUT3} (Pins E11, F11), V_{OUT4} (Pins B11, C11), V_{OUT5} (Pins A10, A11): These are the power outputs of the individual LDOs. There must be a minimum load current of 1mA or the output may not regulate. The internal LDOs are rated for positive voltages between their inputs and outputs. Avoid applications where the internal LDOs can experience a negative voltage, even during start-up and turn-off transients.

BLOCK DIAGRAM



OPERATION

The LTM8001 consists of two major parts: the first is a standalone nonisolated step-down switching DC/DC power converter that can deliver up to 5A of output current. The second part is an array of five parallelable 1.1A LDOs. The DC/DC converter provides a precisely regulated output voltage programmable via one external resistor from 1.2V to 24V. The input voltage range is 6V to 36V. Given that it is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. The linear regulator array consists of five low drop-out regulators, of which three inputs are dedicated to the buck converter's output (V_{OUT0}) and two tie to an undedicated input (V_{IN45}). Each individual linear regulator may be set to a unique voltage through its SET pin, or may be paralleled with other LDOs by tying their respective SET and V_{OUT} pins together.

The LTM8001 step-down switching converter utilizes fixed frequency, average current mode control to accurately regulate the output current. This results in a constant-voltage, constant-current output characteristic, making the LTM8001's step-down regulator well suited for many supercapacitor and battery charging applications. As shown in the Typical Performance Characteristics, the current limit works in both directions. The control loop will regulate the current in the internal inductor. Once the V_{OUT0} output has reached the regulation voltage determined by the resistor from the FBO pin to ground, the voltage regulation loop will reduce the output current and maintain the output voltage. The ILIM input may be used to set the maximum allowable current output of the LTM8001. The analog control range of the ILIM pin is from 0V to 1.5V. If the ILIM pin is raised above 1.5V, there is little or no effect.

The RUN pin functions as a precision enable for the step-down switching converter connected to V_{OUT0}. If all V_{OUT1-3} LDO inputs including BIAS are tied to V_{OUT0}, the RUN pin will also implicitly enable or disable these LDOs as well. If an external power source is applied to BIAS123 alone or in combination with V_{OUT0}, RUN will not disable V_{OUT1-3}. Refer to the Applications Information section Shorted Input Protection if V_{OUT0} is forced above V_{IN0}. When the voltage at the RUN pin is lower than 1.55V, switching is terminated. Below the turn-on threshold, the RUN pin sinks 5.5µA. This current can be used with a resistor between RUN and V_{IN0} to set hysteresis. Please refer to the UVLO and Shutdown section in the Applications Information for further details. During start-up, the SS pin is held low until the part is enabled, after which the capacitor at the soft-start pin is charged with an 11µA current source.

The LTM8001 is equipped with thermal shutdown circuitry to protect the device during momentary overload conditions. It is set above the 125°C absolute maximum internal temperature rating to avoid interfering with normal specified operation, so internal device temperatures will exceed the absolute maximum rating when the over-temperature protection is active. Thus, continuous or repeated activation of the thermal shutdown may impair device reliability. During thermal shutdown, all switching is terminated and the SS pin is driven low.

The switching frequency is determined by a resistor at the RT pin. The LTM8001 may also be synchronized to an external clock through the use of the SYNC pin. Please see the Switching Frequency Synchronization section in the Applications Information for further details.

The V_{OUT1-5} linear regulators are easy to use and have all the protection features expected in high performance regulators. Included are short-circuit protection and safe operating area protection, as well as thermal shutdown. These linear regulators are especially well suited to applications needing multiple rails. Their architecture allows their outputs to be adjusted down to zero volts. The output voltage is set by a single resistor, handling modern low voltage digital ICs as well as allowing easy parallel operation and simplified thermal management.

The linear regulators can be operated in two modes. One mode has the BIAS123 and BIAS45 pins connected to the linear regulator power input pins (V_{OUT0} and V_{IN45}) which gives a limitation of about 1.6V dropout. In the other mode, the BIAS123 and BIAS45 pins can be tied to a voltage at least 1.6V above their highest respective outputs. The linear regulator power input (V_{OUT0} and V_{IN45}) can then be set to a lower voltage that meets the dropout requirement, minimizing the power dissipation.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and V_{OUT0} output voltage.
2. Apply the recommended C_{IN0}, C_{OUT0}, R_{FB0} and R_T values. Note that ceramic and electrolytic capacitors are recommended. These are intended to work in concert to optimize performance and solution size; apply both capacitors.
3. Apply the set resistors for the V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4} and V_{OUT5} regulators. To set the voltage of each linear regulator, use the equation

$$R_{SETX} = \frac{V_{OUTX}}{10\mu A}$$

where the value of R_{SET} is in Ohms. Note that there is no minimum positive output voltage for the regulator, but a minimum load current is required to maintain regulation regardless of output voltage, (please see Electrical Characteristics table). For true zero voltage output operation, this minimum load current must be returned to a negative supply voltage. If paralleling the linear regulators, set the output of each regulator to the same voltage by tying the SETx pins together and applying a single resistor. The value of the single set resistor is given by the equation:

$$R_{SET} = \frac{V_{OUT}}{10\mu A \bullet n}$$

where n is the number of regulators paralleled.

4. Apply the output capacitors for the V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4} and V_{OUT5} regulators. A minimum output capacitor of 2.2µF with an ESR of 0.5Ω or less is recommended to prevent oscillations.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8001 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Switching Frequency Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature, applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected. Many of the output capacitances given in Table 1 specify an electrolytic capacitor. Ceramic capacitors may also be used in the application, but it may be necessary to use more of them. Many high value ceramic capacitors have a large voltage coefficient, so the actual capacitance of the component at the desired operating voltage may be only a fraction of the specified value. Also, the very low ESR of ceramic capacitors may necessitate additional capacitors for acceptable stability margin.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8001. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8001 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot Plugging Safely section.

APPLICATIONS INFORMATION

Table 1. LTM8001 Recommended Component Values and Configuration for V_{OUT0} (T_A = 25°C)

V_{IN0}	V_{OUT0}	C_{IN0}	C_{OUT0} (CERAMIC)	C_{OUT0} (ELECTROLYTIC)	R_{FB0}	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
6V to 36V	1.2V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	Open	200kHz	200k	250kHz	169k
6V to 36V	1.5V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	38.3k	300kHz	140k	350kHz	118k
6V to 36V	1.8V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	19.6k	350kHz	118k	400kHz	102k
6V to 36V	2.5V	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	9.09k	450kHz	90.9k	525kHz	78.7k
6V to 36V	3.3V	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	625kHz	64.9k
7V to 36V	5V	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	700kHz	57.6k
10V to 36V	8V	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	750kHz	53.6k
15V to 36V	12V	10µF, 50V, 1210	47µF, 16V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.10k	650kHz	61.9k	800kHz	49.9k
22V to 36V	18V	10µF, 50V, 1210	22µF, 25V, 1210	47µF, 20V, 45mΩ, OS-CON, 20SVPS47M	715Ω	675kHz	59.0k	900kHz	44.2k
28V to 36V	24V	4.7µF, 50V, 1210	10µF, 50V, 1206	47µF, 35V, 30mΩ, OS-CON, 35SVPC47M	523Ω	700kHz	57.6k	1MHz	39.2k
9V to 15V	1.2V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	Open	200kHz	200k	525kHz	78.7k
9V to 15V	1.5V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	38.3k	300kHz	140k	650kHz	61.9k
9V to 15V	1.8V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	19.6k	350kHz	118k	800kHz	49.9k
9V to 15V	2.5V	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	9.09k	450kHz	90.9k	1MHz	39.2k
9V to 15V	3.3V	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	1MHz	39.2k
9V to 15V	5V	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	1MHz	39.2k
10V to 15V	8V	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	1MHz	39.2k
18V to 36V	1.2V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	Open	200kHz	200k	250kHz	169k
18V to 36V	1.5V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	38.3k	300kHz	140k	350kHz	118k
18V to 36V	1.8V	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	19.6k	350kHz	118k	400kHz	102k
18V to 36V	2.5V	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	9.09k	450kHz	90.9k	525kHz	78.7k
18V to 36V	3.3	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	625kHz	64.9k
18V to 36V	5V	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	700kHz	57.6k
18V to 36V	8V	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	750kHz	53.6k
18V to 36V	12V	10µF, 50V, 1210	47µF, 16V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.10k	650kHz	61.9k	800kHz	49.9k

Note: An input bulk capacitor is required.

APPLICATIONS INFORMATION

Programming Switching Frequency

The LTM8001 has an operational switching frequency range between 200kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. See Table 2 for resistor values and the corresponding switching frequencies.

Table 2. R_T Resistor Values and Their Resultant Switching Frequencies

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
1	39.2
0.75	53.6
0.5	82.5
0.3	140
0.2	200

Switching Frequency Trade-Offs

It is recommended that the user apply the optimal R_T resistor value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8001 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8001 in some fault conditions. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Switching Frequency Synchronization

The nominal switching frequency of the LTM8001 is determined by the resistor from the RT pin to GND and may be set from 200kHz to 1MHz. The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 0.8V and a logic high greater than 1.2V. The input frequency must be 20% higher than the frequency determined by the resistor at the RT pin. The SYNC pin must be tied to GND if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor at the RT pin.

Soft-Start

The soft-start function controls the slew rate of the power supply output V_{OUT0} voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN0} supply, and facilitates supply sequencing. A capacitor connected from the SS pin to GND programs the slew rate. The capacitor is charged from an internal 11µA current source to produce a ramped output voltage.

Maximum Output Current Adjust

The LTM8001 features an adjustable accurate current limit. To adjust the load current limit, an analog voltage is applied to the ILIM pin. Varying the voltage between 0V and 1.5V adjusts the maximum current between the minimum and the maximum current, 5.6A typical. Above 1.5V, the control voltage has no effect on the regulated inductor current. Graphs of the output current vs ILIM voltages are given in the Typical Performance Characteristics section. The LTM8001 provides a 2V reference voltage for conveniently applying resistive dividers to set the current limit. The current limit can be set as shown in Figure 1 with the following equation:

$$I_{MAX} = 7.47 \frac{R2}{R1+R2}$$

A convenient value of R1 may be 10k. In that case,

$$R2 = \frac{10 \bullet I_{MAX}}{7.47 - I_{MAX}}\ k\Omega$$

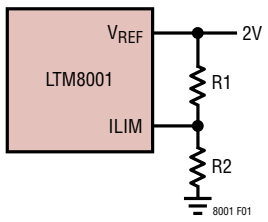


Figure 1. Setting the Output Current Limit, I_{MAX}

APPLICATIONS INFORMATION

Load Current Derating Using the ILIM Pin

In high current applications, derating the maximum current based on operating temperature may prevent damage to the load. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on the load and/or board temperature. To achieve this, the LTM8001 uses the ILIM pin to reduce the effective regulated current in the load. While ILIM programs the regulated current in the load, it may also be configured to reduce the regulated current. The load/board temperature derating is programmed using a resistor divider with a temperature dependant resistance, as shown in Figure 2. When the board/load temperature rises, the ILIM voltage will decrease.

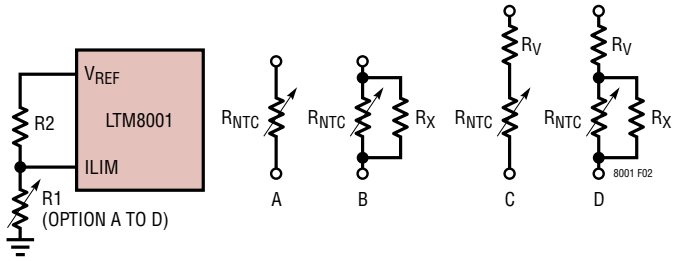


Figure 2. Load Current Derating vs Temperature Using an NTC Resistor

V_{OUT0} Output Overvoltage Protection

The LTM8001 switching regulator uses the FB0 pin to both regulate the output voltage and to provide a high speed overvoltage lockout to avoid high voltage output conditions. If the output voltage exceeds 125% of the regulated voltage level (1.5V at the FB0 pin), the LTM8001 terminates switching and shuts down switching for a brief period. The output voltage at which output overvoltage protection engages must be greater than 1.5V and is set by the equation:

$$V_{OUT} = 1.5V\left(1+\frac{10k}{R_{FB0}}\right)$$

where R_{FB0} is shown in Figure 3.

If the output overvoltage protection engages, the LTM8001 will stop switching. If this is due to some external power source connected to V_{OUT0}, this source will be free to pull up V_{OUT0}. If the V_{OUT0} voltage exceeds the V_{IN0} input, an internal power diode will clamp the output to a diode drop above the input.

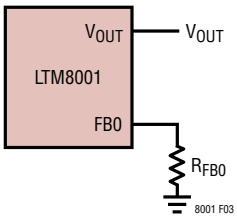


Figure 3. Voltage Regulation and Overvoltage Protection Feedback Connections

Thermal Shutdown

If the part is too hot, the LTM8001 engages its thermal shutdown, terminates switching and discharges the soft-start capacitor. When the part has cooled, the part automatically restarts. This thermal shutdown is set to engage at temperatures above the 125°C absolute maximum internal operating rating to ensure that it does not interfere with functionality in the specified operating range. This means that internal temperatures will exceed the 125°C absolute maximum rating when the overtemperature protection is active, possibly impairing the device's reliability.

UVLO and Shutdown

The LTM8001 V_{OUT0} step-down regulator has an internal UVLO that terminates switching, resets all logic, and discharges the soft-start capacitor for input voltages below 4.2V. The LTM8001 also has a precision RUN function that enables switching when the voltage at the RUN pin rises to 1.68V. Partial shutdown occurs at 1.55V and full shutdown is guaranteed below 0.5V with <1µA I_Q in the full shutdown state. There is also an internal current source that provides 5.5µA of pull-down current to program additional UVLO hysteresis. For RUN rising, the current source is sinking 5.5µA until RUN = 1.68V, after which it turns off. For RUN falling, the current source is off until the RUN = 1.55V, after which it sinks 5.5µA. The following equations determine the voltage divider resistors for programming the falling UVLO voltage and rising enable voltage (V_{ENA}) as configured in Figure 4.

$$R2 = \frac{V_{ENA} - 1.084\ UVLO}{5.5\mu A}$$

$$R1 = \frac{1.55\ R2}{UVLO - 1.55}$$

APPLICATIONS INFORMATION

The RUN pin has an absolute maximum voltage of 6V. To accommodate the largest range of applications, there is an internal Zener diode that clamps this pin, so that it can be pulled up to a voltage higher than 6V through a resistor that limits the current to less than 100µA. For applications where the supply range is greater than 4:1, size R2 greater than 375k.

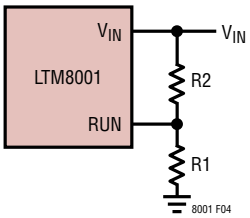


Figure 4. UVLO Configuration

Load Sharing

The V_{OUT0} step-down switching converter operates in fixed frequency forced continuous mode, so it is able to source and sink current. It is therefore not suitable for load current sharing.

The linear regulators connected to V_{OUT1}-V_{OUT5} are internally ballasted and may be paralleled. To do this, simply tie the V_{OUTx} and SETx terminals together. When the SET pins of the regulators are tied together, the R_{SET} resistor is determined by the equation:

$$R_{SET} = \frac{V_{OUT}}{n \bullet 10\mu A}$$

where n is the number of linear regulator outputs tied together.

All paralleled LDOs must be active in order for this equation to be true, as it is assumed that all paralleled LDOs are contributing 10µA to a single voltage set resistor. If any LDO is off or inactive, it will be unable to contribution its share of the set current and the output voltage will be lower than expected.

When paralleling LDOs, tie all of the V_{OUTx} and all of the SETx pins together. Examples are shown in the Typical Applications section.

Input Precautions

The LTM8001 contains a step-down switching regulator that operates at a user-selectable frequency in forced continuous mode. Step-down switching regulators that operate in forced continuous mode are capable of both sinking and sourcing current to maintain output voltage regulation

When the LTM8001 is sinking current, it maintains its output voltage regulation by power conversion, not power dissipation. This means that the energy provided to the LTM8001 is in turn delivered to its input power bus. There must be something on this power bus to accept or use the energy, or the LTM8001's input voltage will rise. Left unchecked, the energy can raise the input voltage above the absolute maximum voltage rating and damage the LTM8001.

In many cases, the system load on the LTM8001 input bus will be sufficient to absorb the energy delivered by the µModule regulator. The power required by other devices will consume more than enough to make up for what the LTM8001 delivers. In cases where the LTM8001 is the largest or only power converter, this may not be true and some means may need to be devised to prevent the LTM8001's input from rising too high. Figure 5a shows a passive crowbar circuit that will dissipate energy during momentary input overvoltage conditions. The breakdown voltage of the zener diode is chosen in conjunction with the resistor R to set the circuit's trip point. The trip point is typically set well above the maximum V_{IN} voltage under normal operating conditions. This circuit does not have a precision threshold, and is subject to both part-to-part and temperature variations, so it is not suitable for applications where high accuracy is required or large voltage margins are not available.

The circuit in Figure 5b also dissipates energy during momentary overvoltage conditions, but is more precise than that in Figure 5a. It uses an inexpensive comparator and the V_{REF} output of the LTM8001 to establish a reference voltage. The optional hysteresis resistor in the comparator circuit avoids MOSFET chatter. Figure 5c shows a circuit that latches on and crowbars the input in an

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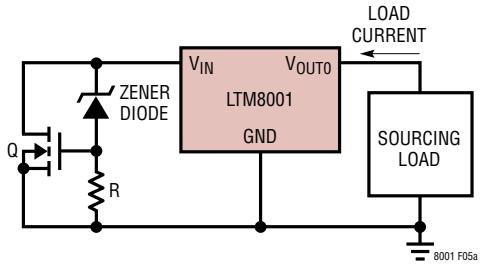
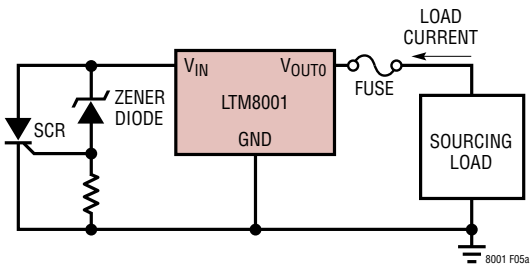
overvoltage event. The SCR latches when the input voltage threshold is exceeded, so this circuit should be used with a fuse, as shown, or employ some other method to interrupt current from the load.

As mentioned, the LTM8001 sinks current by energy conversion and not dissipation. Thus, no matter what protection circuit that is used, the amount of power that the protection circuit must absorb depends upon the amount of power at the input. For example, if the output voltage is 2.5V and can sink 5A, the input protection circuit should be designed to absorb at least 7.5W. In Figure 5a and Figure 5b, let us say that the protection activation threshold is 30V. Then the circuit must be designed to be able to dissipate 7.5W and accept 7.5W/30V = 250mA.

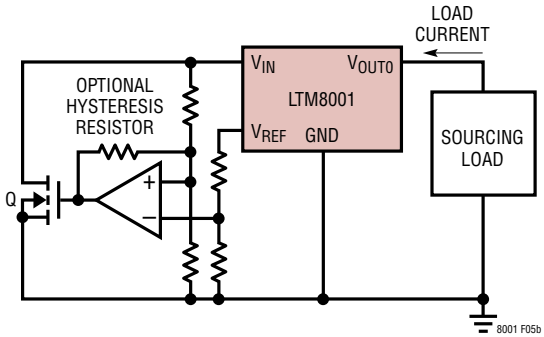
Figure 5a through Figure 5c are crowbar circuits, which attempt to prevent the input voltage from rising above some level by clamping the input to GND through a power device. In some cases, it is possible to simply turn off the LTM8001 when the input voltage exceeds some threshold. This is possible when the voltage power source that drives current into V_{OUT} never exceeds V_{IN}. An example of this circuit is shown in Figure 5d. When the power source on the output drives V_{IN} above a predetermined threshold, the comparator pulls down on the RUN pin and stops switching in the LTM8001. When this happens, the input capacitance needs to absorb the energy stored within the LTM8001's internal inductor, resulting in an additional voltage rise. As shown in the Block Diagram, the internal



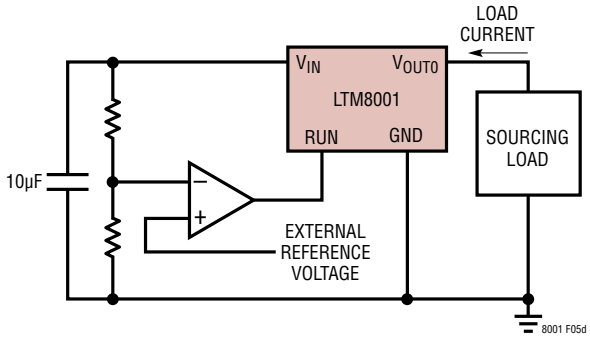
(5a) The MOSFET Q Dissipates Momentary Energy to GND. The Zener Diode and Resistor Are Chosen to Ensure That the MOSFET Turns On Above the Maximum V_{IN} Voltage Under Normal Operation



(5c) The SCR Latches On When the Activation Threshold is Reached, So a Fuse or Some Other Method of Disconnecting the Load Should be Used



(5b) The Comparator in This Circuit Activates the Q MOSFET at a More Precise Voltage Than the One Shown in Figure 5a. The Reference for the Comparator is Derived from the V_{REF} Pin of the LTM8001



(5d) This Comparator Circuit Turns Off the LTM8001 if the Input Rises Above a Predetermined Threshold. When the LTM8001 Turns Off, the Energy Stored in the Internal Inductor Will Raise V_{IN} a Small Amount Above the Threshold.

Figure 5. Crowbar Circuits

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inductor value is 2.2uH. If the LTM8001 negative current limit is set to 5A, for example, the energy that the input capacitance must absorb is 1/2 LI^2 = 27.5µJ. Suppose the comparator circuit in Figure 5d is set to pull the RUN pin down when V_{TRIP} = 15V. The input voltage will rise according to the capacitor energy equation:

$$\frac{1}{2}C\left(V_{IN}^2 - V_{TRIP}^2\right) = 27.5\mu J$$

If the total input capacitance is 10µF, the input voltage will rise to:

$$27.5\mu J = \frac{1}{2}10\mu F\left(V_{IN}^2 - 15V^2\right)$$

V_{IN} = 15.2V

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8001. The LTM8001 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 6 for a suggested layout. Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the R_{SETx}, R_{FB0} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN0} capacitor as close as possible to the V_{IN0} and GND connection of the LTM8001.
3. Place the ceramic C_{OUT0} capacitor as close as possible to the V_{OUT0} and GND connection of the LTM8001. The electrolytic C_{OUT0} capacitor may be farther from the LTM8001. Place the remaining C_{OUTx} output capacitors as close as possible to the V_{OUTx} pins.
4. Place the C_{IN0} and C_{OUT0} capacitors such that their ground currents flow directly adjacent or underneath the LTM8001.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8001.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 6. The LTM8001 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

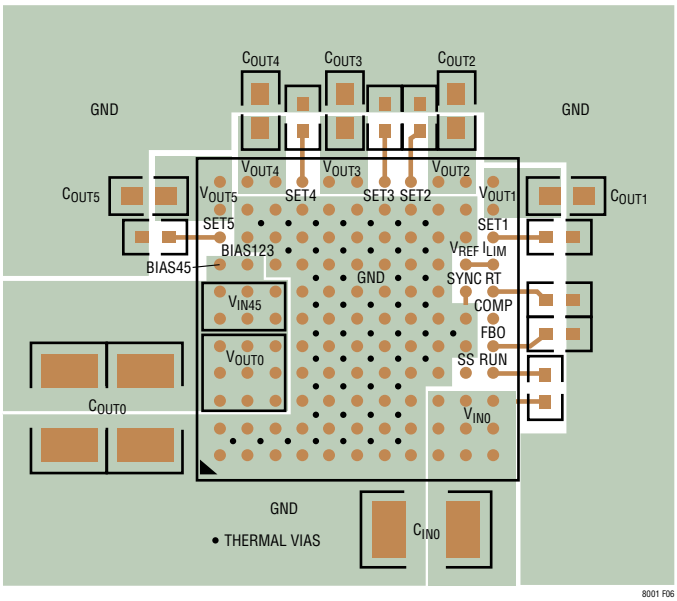

Figure 6. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8001. However, these capacitors can cause problems if the LTM8001 is plugged into a live input supply (see Analog Devices Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN0} pin of the LTM8001 can ring to more than twice the nominal input voltage, possibly exceeding

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the LTM8001's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8001 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN0}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN0} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the performance of the circuit, though it may be physically large.

Shorted Input Protection

Care needs to be taken in systems where the V_{OUT0} output will be held high when the input to the LTM8001 is absent. If the V_{IN0} is allowed to float and the RUN pin is held high (either by a logic signal or because it is tied to V_{IN0}), then the LTM8001's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate this state. If the RUN pin is pulled low, the input current will drop to essentially zero. However, if the V_{IN0} is grounded while the V_{OUT0} output is held high, then parasitic diodes inside the LTM8001 can pull large currents from the output through the V_{IN0} pin. Figure 7 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

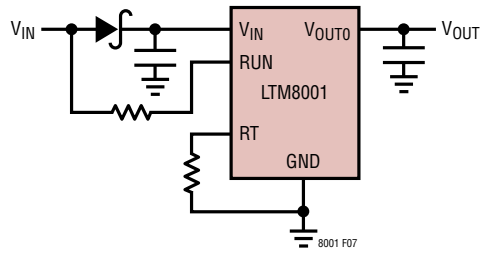


Figure 7. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8001 Runs Only When the Input is Present

Charging Applications

The LTM8001's internal switching step-down regulator's CVCC operation makes it well suited for battery or supercapacitor charging applications. A schematic of the LTM8001 charging a supercapacitor and then distributing power to various loads through the onboard LDOs is shown in the Typical Applications section. In this application, the supercapacitor is charged through the step-down switching regulator and not the LDOs. Each LDO is rated for positive and differential voltages between its input and output, but may experience a negative voltage during start-up or turn-off transients if its output is connected to a battery, supercapacitor or energized load. Avoid using the LTM8001 in applications where the internal LDOs can experience a negative voltage.

Thermal Considerations

The LTM8001 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8001 mounted to a $59cm^2$ 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. To that end, the Pin Configuration of this data sheet typically gives four thermal coefficients:

θ_{JA}: Thermal resistance from junction to ambient

$\theta_{JCbottom}$: Thermal resistance from junction to the bottom of the product case

θ_{JCtop}: Thermal resistance from junction to top of the product case

θ_{JB}: Thermal resistance from junction to the printed circuit board

APPLICATIONS INFORMATION

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in this product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is Figure 8. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8001 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8001. The bulk of the heat flow out of the LTM8001 is through the bottom of the module and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

APPLICATIONS INFORMATION

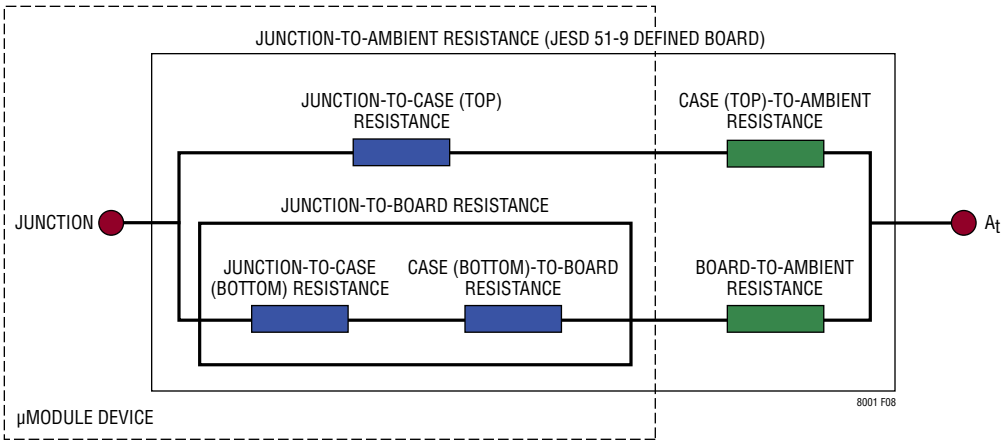
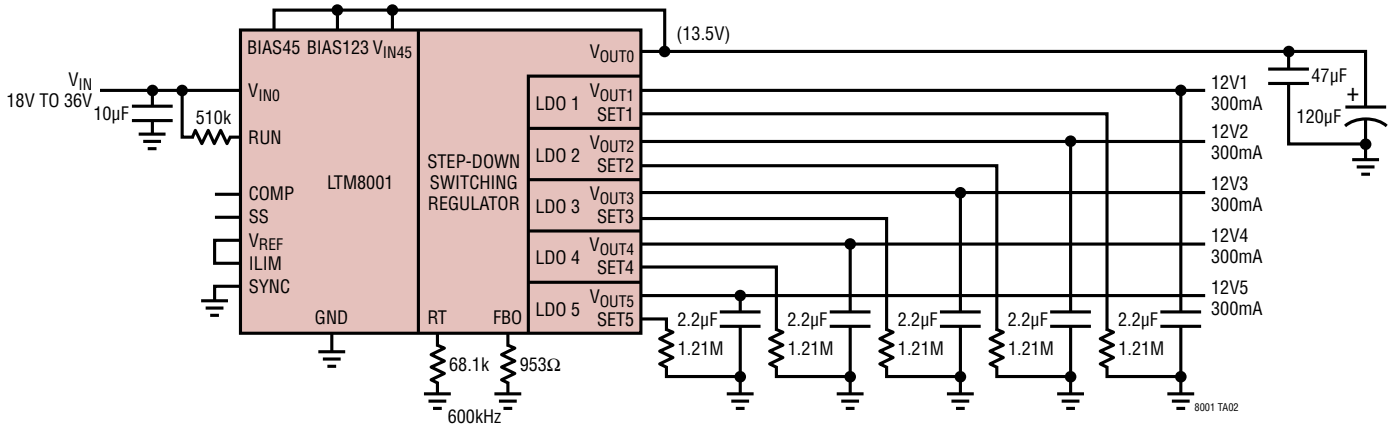


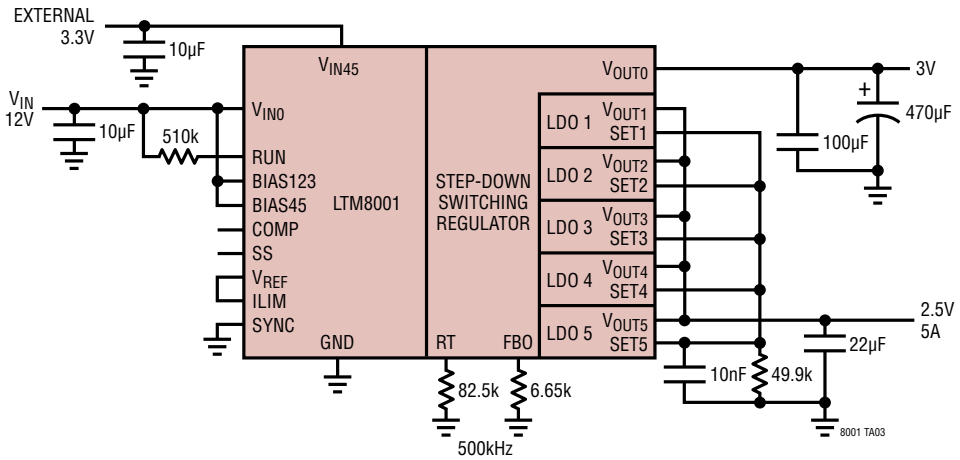
Figure 8. Thermal Resistances Among µModule Device Printed Circuit Board and Ambient Environment

TYPICAL APPLICATIONS

Five Output DC/DC µModule Regulator

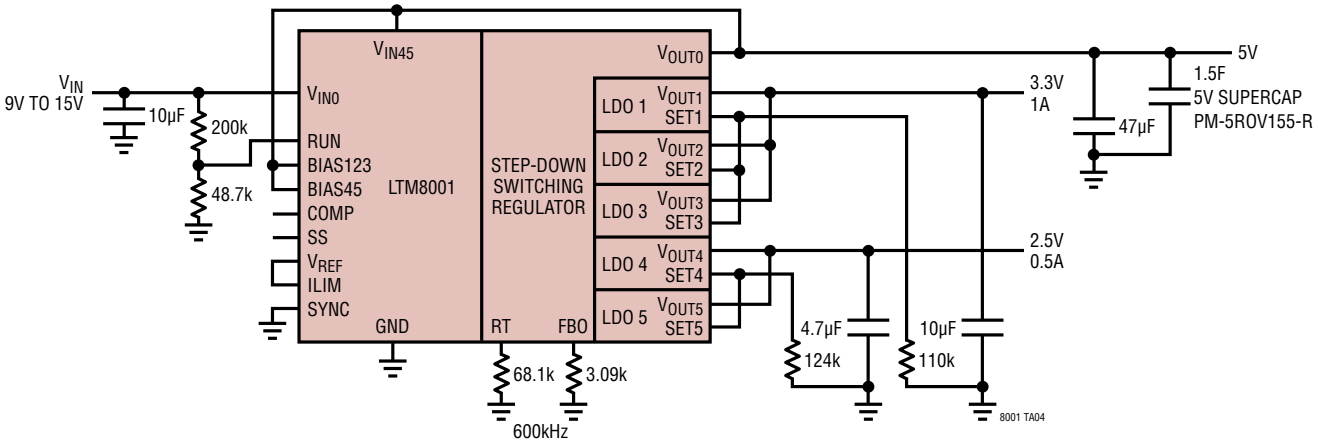


Dual Input, 2.5V 5A DC/DC µModule Converter Using a Single LTM8001
(External 3.3V Turns On Before or Simultaneously with 12V)



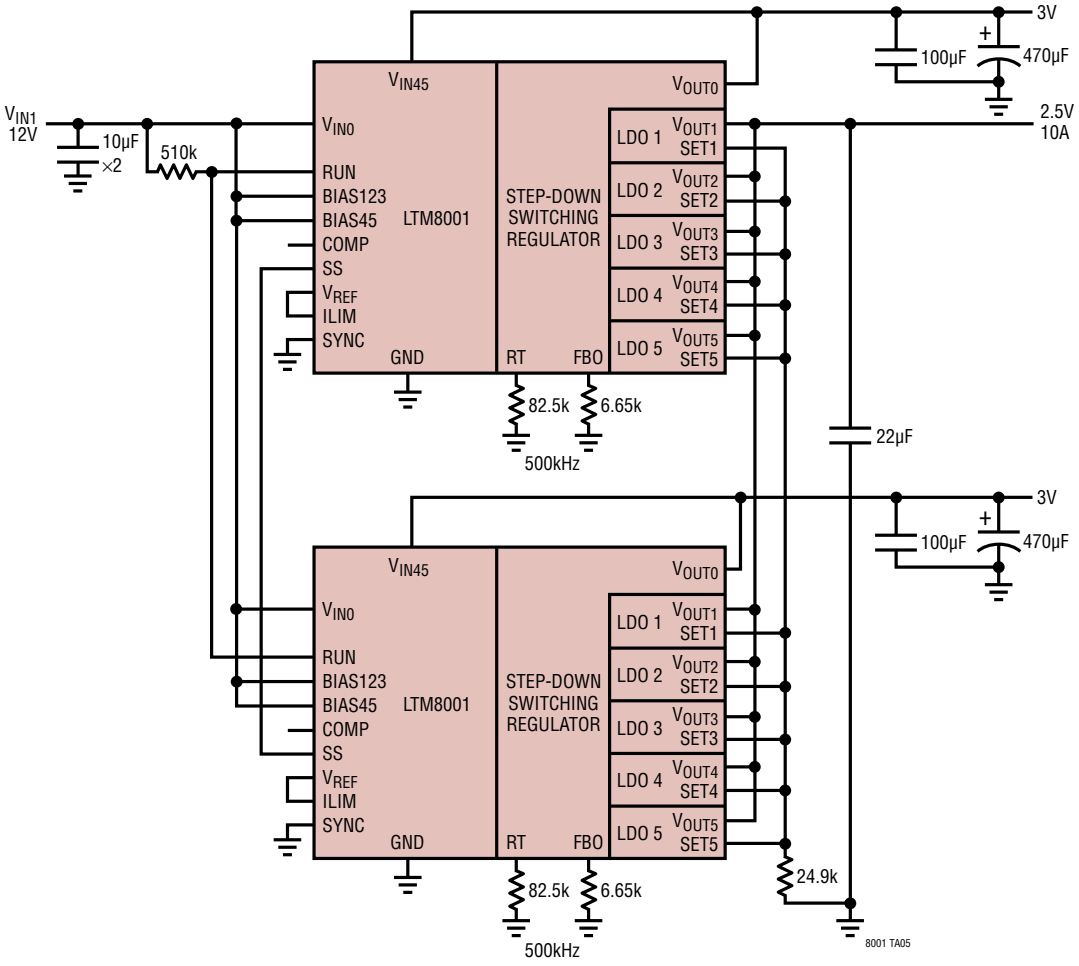
TYPICAL APPLICATIONS

Supercapacitor Charger and Two Output Regulator

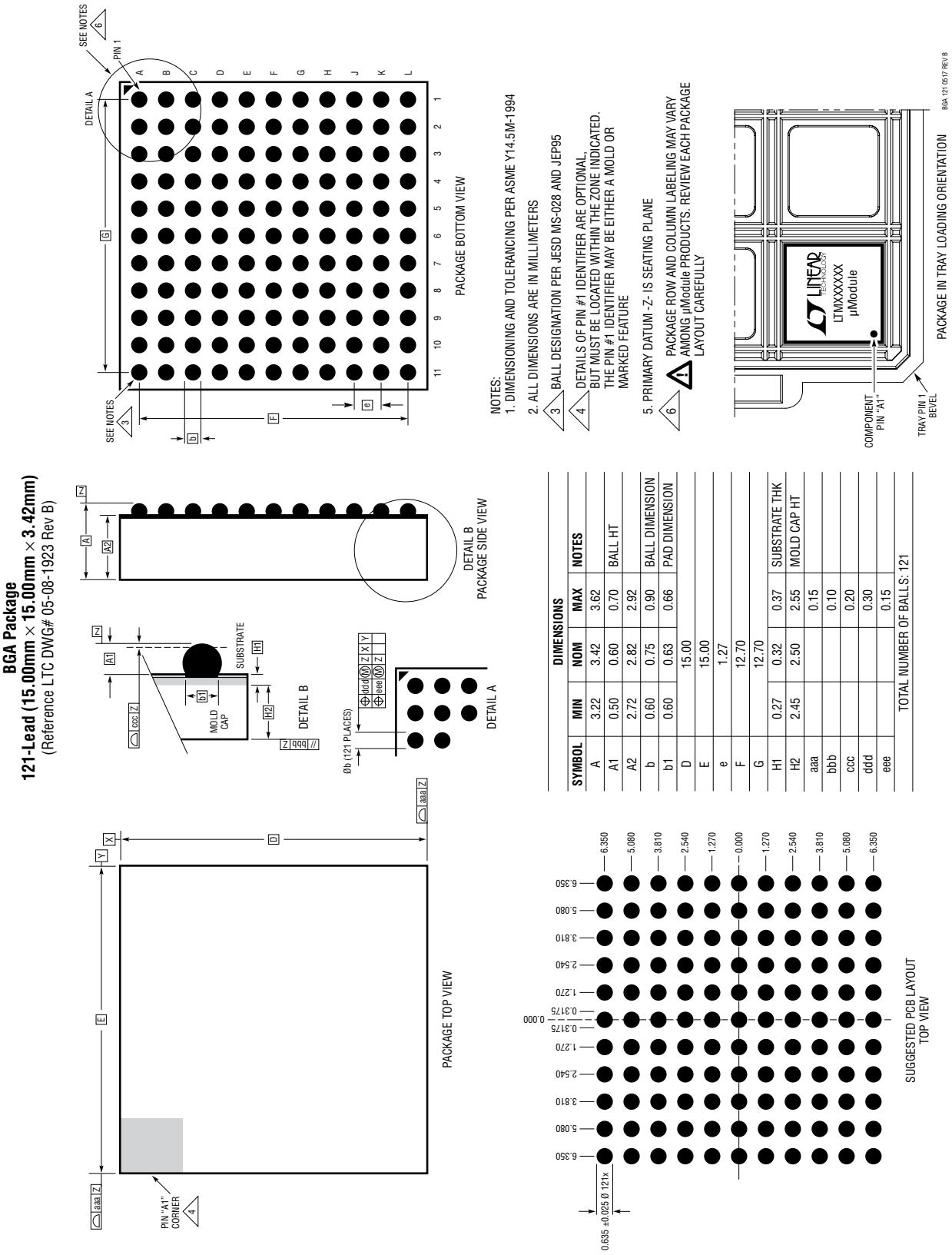


TYPICAL APPLICATIONS

Use Two LTM8001s to Implement a 2.5V_{OUT} 10A DC/DC µModule Converter



PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	BALL HT
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		15.00		
e		1.27		
F		12.70		
G		12.70		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	2.45	2.50	2.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 121				

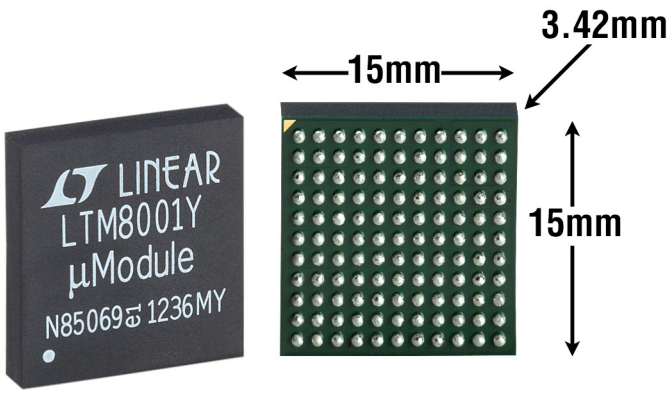
PACKAGE DESCRIPTION

Table 3. LTM8001 Pinout (Sorted by Pin Number)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	GND	B1	GND	C1	GND	D1	GND	E1	GND	F1	GND
A2	GND	B2	GND	C2	GND	D2	GND	E2	GND	F2	GND
A3	V_{OUT0}	B3	V_{OUT0}	C3	V_{OUT0}	D3	GND	E3	GND	F3	GND
A4	V_{OUT0}	B4	V_{OUT0}	C4	V_{OUT0}	D4	GND	E4	GND	F4	GND
A5	V_{OUT0}	B5	V_{OUT0}	C5	V_{OUT0}	D5	GND	E5	GND	F5	GND
A6	V_{IN45}	B6	V_{IN45}	C6	V_{IN45}	D6	GND	E6	GND	F6	GND
A7	V_{IN45}	B7	V_{IN45}	C7	V_{IN45}	D7	GND	E7	GND	F7	GND
A8	BIAS45	B8	BIAS123	C8	GND	D8	GND	E8	GND	F8	GND
A9	SET5	B9	GND	C9	GND	D9	GND	E9	GND	F9	GND
A10	V_{OUT5}	B10	GND	C10	GND	D10	GND	E10	GND	F10	GND
A11	V_{OUT5}	B11	V_{OUT4}	C11	V_{OUT4}	D11	SET4	E11	V_{OUT3}	F11	V_{OUT3}

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
G1	GND	H1	GND	J1	V_{IN0}	K1	V_{IN0}	L1	V_{IN0}
G2	GND	H2	GND	J2	V_{IN0}	K2	V_{IN0}	L2	V_{IN0}
G3	GND	H3	GND	J3	V_{IN0}	K3	V_{IN0}	L3	V_{IN0}
G4	GND	H4	GND	J4	GND	K4	SS	L4	RUN
G5	GND	H5	GND	J5	GND	K5	GND	L5	FB0
G6	GND	H6	GND	J6	GND	K6	GND	L6	COMP
G7	GND	H7	GND	J7	GND	K7	SYNC	L7	RT
G8	GND	H8	GND	J8	GND	K8	V_{REF}	L8	ILIM
G9	GND	H9	GND	J9	GND	K9	GND	L9	SET1
G10	GND	H10	GND	J10	GND	K10	GND	L10	V_{OUT1}
G11	SET3	H11	SET2	J11	V_{OUT2}	K11	V_{OUT2}	L11	V_{OUT1}

PACKAGE PHOTO

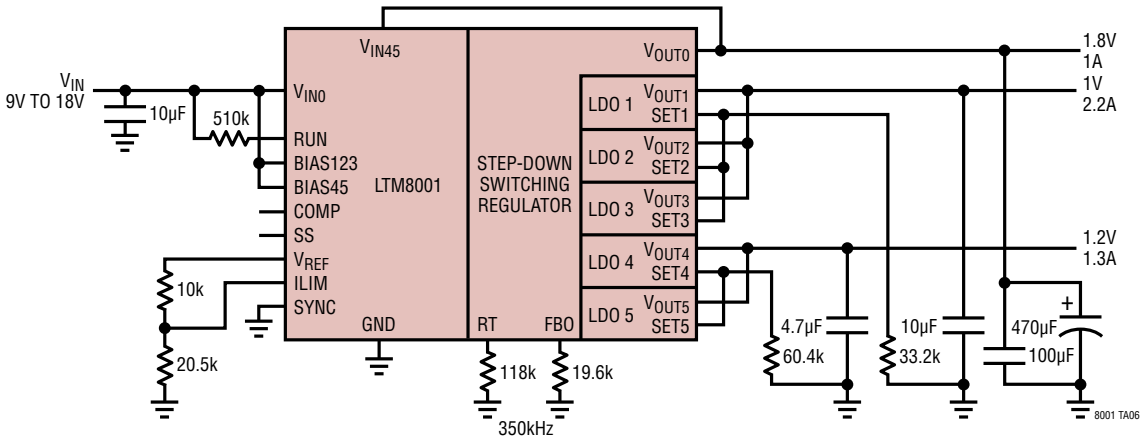


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/13	Update Features section	1
		Update test conditions and limits	3, 4
		Correct input power pin name	11
B	02/14	Add SnPb BGA package option	1, 2
C	08/14	Add MP-grade option	2, 3
D	08/15	Modified maximum V_{OUT} conditions	4
		Amended V_{OUT} RUN description	11
E	12/20	Corrected Pin Configuration to JESD	2
		Added switching frequency to the titles of G01–G07	4, 5
		Updated V_{FB} resistor to ±1% in Block Diagram	10
		Corrected UVLO and Shutdown section	15

TYPICAL APPLICATION

Three Output DC/DC µModule Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8026	36V_{IN}, 5A Step-Down µModule Regulator with Adjustable Current Limit	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, Adjustable Current Limit, Parallelable Outputs, CLK Input, 11.25mm × 15mm × 2.82mm LGA
LTM8052	36V_{IN}, ±5A Step-Down µModule Regulator with Adjustable Current Limit	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, –5V ≤ I_{OUT} ≤ 5A, Adjustable Current Limit, CLK Input, 11.25mm × 15mm × 2.82mm LGA, Pin Compatible with LTM8026
LTM8061	32V, 2A Step-Down µModule Battery Charger with Programmable Input Current Limit	Suitable for CC-CV Charging Single and Dual Cell Li-Ion or Li-Poly Batteries, 4.95V ≤ V_{IN} ≤ 32V, C/10 or Adjustable Timer Charge Termination, NTC Resistor Monitor Input, 9mm × 15mm × 4.32mm LGA
LTM8062A	32V, 2A Step-Down µModule Battery Charger with Integrated Maximum Peak Power Tracking (MPPT) for Solar applications	Suitable for CC-CV Charging Method Battery Chemistries (Li-Ion, Li-Poly, Lead-Acid, $LiFePO_4$), User Adjustable MPPT Servo Voltage, 4.95V ≤ V_{IN} ≤ 32V, 3.3V ≤ V_{BATT} ≤ 18.8V Adjustable, C/10 or Adjustable Timer Charge Termination, NTC Resistor Monitor Input, 9mm × 15mm × 4.32mm LGA
LTM8033	36V, 3A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 24V, Synchronizable, 11.25mm × 15mm × 4.32mm LGA
LTM4613	36V_{IN}, 8A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, PLL input, V_{OUT} Tracking and Margining, 15mm × 15mm × 4.32mm LGA
LTM8048	1.5W, 725VDC Galvanically Isolated µModule Converter with LDO Post regulator	3.1V ≤ V_{IN} ≤ 32V, 2.5V ≤ V_{OUT} ≤ 12V, 1mV_{P-P} Output Ripple, Internal Isolated Transformer, 9mm × 11.25mm × 4.92mm BGA
LTC®2978	Octal Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, 16-Bit ADC with ±0.25% TUE, 3.3V to 15V Operation
LTC2974	Quad Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, per Channel Voltage, Current and Temperature Measurements
LTC3880	Dual Output PolyPhase® Step-Down DC/DC Controller with Digital Power System Management	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, ±0.5% Output Voltage Accuracy, MOSFET Gate Drivers